an oxide layer to be measured located above a body of doped semiconductor material and arranged in a position adjacent to a gate region of polycrystalline semiconductor material, said oxide layer having a first area;

an oxide test region of the same material as said oxide layer and having the same thickness and the same electrical characteristics as said oxide layer;

a field oxide region separating the oxide test region from the oxide layer; and

a polycrystalline region of the same material as said gate region, having the same thickness and the same electrical characteristics as said gate region, and positioned adjacent to the oxide test region, said oxide test region having a second area greater than the first area.

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2. (Amended) A structure according to claim 1 wherein said polycrystalline region has a closed perimeter that completely surrounds a central opening in the polycrystalline region.

3. A structure according to claim 2 wherein said closed line delimits an area with dimensions greater than 50x50 μm^2.

4. (Amended) The structure according to claim 1 wherein said polycrystalline region laterally completely surrounds and delimits said oxide test region.

5. (Amended) A structure for checking an integrated electronic device, comprising:

a doped semiconductor material body;

a gate region of polycrystalline semiconductor material;

an oxide layer having a thickness to be determined, located the semiconductor material body, arranged in a position adjacent to the gate region, and having a first area; and

a test region positioned on the semiconductor material body, the test region including an oxide test region of a same material as the oxide layer and having a thickness that is equal to the thickness of the oxide layer, the oxide test region having a second area that is greater than the first area and sufficiently large to be measured in a non-destructive manner by an

ellipsometer, wherein the test region further includes a polycrystalline region that completely surrounds the oxide test region.

6. (Amended) The structure of claim 5 wherein the oxide layer overlies a first active region of the semiconductor material body and the oxide test region overlies a second active region of the semiconductor material body.

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7. (Amended) The test structure of claim 5 wherein the polycrystalline region has a closed perimeter that completely surrounds a central opening in the polycrystalline region.

8. The test structure of claim 5 wherein the second area has dimensions greater than or equal to 50x50 μm^2.

Please add new claims 9-20 to read as follows:

a2 9. A structure for checking an integrated electronic device, comprising:

a doped semiconductor material body;

a gate region of polycrystalline semiconductor material;

a dielectric layer having a thickness to be determined, located on the semiconductor material body, arranged in a position adjacent to the gate region, and having a first area; and

a test region positioned on the semiconductor material body, the test region including a dielectric test region and a polycrystalline region, the polycrystalline region being of the same semiconductor material as the gate region and completely laterally surrounding the dielectric test region, the dielectric test region being of a same material as the dielectric layer and having a thickness that is equal to the thickness of the dielectric layer, the dielectric test region having a second area that is greater than the first area and being positioned directly on the semiconductor material body.

10. The structure of claim 9 wherein the dielectric layer overlies a first active region and the test region overlies a second active region.

11. The test structure of claim 9 wherein the polycrystalline region has an interior perimeter that directly contacts the dielectric test region along the entire interior perimeter.

12. The test structure of claim 9 wherein the second area has dimensions greater than or equal to 50x50 μm^2.

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13. The test structure of claim 9 wherein the polycrystalline region has a closed perimeter that completely surrounds a central opening in the polycrystalline region.

14. The test structure of claim 9 wherein the dielectric layer and the dielectric test region are both composed of silicon oxide.

15. A structure for checking an integrated electronic device comprising:

an oxide layer located on a body of doped semiconductor material and arranged in a position adjacent to a gate region of polycrystalline semiconductor material, said oxide layer having a thickness and a first area;

a field oxide region; and

test means for testing the thickness of the oxide layer, the test means including an oxide test region positioned on the body and separated from the oxide layer by the field oxide region.

16. The structure of claim 15 wherein the oxide test region is of the same material as the oxide layer and has the same thickness and the same electrical characteristics as the oxide layer.

17. The structure of claim 15 wherein the test means include a polycrystalline region of the same material as the gate region, the polycrystalline region having the same thickness and the same electrical characteristics as the gate region, and being positioned adjacent to the oxide test region.

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18. The structure according to claim 17 wherein the polycrystalline region laterally completely surrounds and delimits said oxide test region.

19. The structure of claim 17 wherein the polycrystalline region has a closed perimeter that completely surrounds a central opening in the polycrystalline region.

20. The structure of claim 15 wherein said oxide test region has a second area greater than the first area.

REMARKS

Claims 1-20 will be pending upon entry of the present amendment. Claims 2, 4, and 6-7 are being amended. Claims 9-20 are being newly presented.

An embodiment of the invention is directed to an electronic structure that includes an oxide layer, having a thickness desired to be measured, located adjacent to a polysilicon gate region and above a doped semiconductor body. The electronic structure also includes an oxide test region having the same material and thickness as the oxide layer, but with a greater area than the oxide layer. A polycrystalline region laterally surrounds and delimits the oxide test region such that the oxide test region has an area sufficiently large so that the thickness of the oxide test region can be measured by a conventional measuring device such as an ellipsometer. Given that the thickness of the oxide test region equals the thickness of the oxide layer (because both are made according to the same process), the measurement of the thickness of the oxide test regions provides the thickness of the oxide layer.